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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,626	01/24/2002	Andrew Moroney	13453-002001	2191

42178 7590 04/13/2007

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EXAMINER	
SERRAO, RANODHI N	
ART UNIT	**PAPER NUMBER**
2141	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/057,626	MORONEY ET AL.	
	Examiner	Art Unit	
	Ranodhi Serrao	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 and 5-16 have been considered but are moot in view of the new ground(s) of rejection.

2. The applicant argued in substance the newly added limitations of independent claims 1 and 15. However, the new grounds teach these and the added features. See rejections below.

Claim Rejections - 35 USC § 103

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1, 5, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yao et al. (2003/0084219), Satou et al. (5,717,946), and Byers et al. (5,809,543).

6. As per claim 1, Yao et al. teaches a system for enabling communication between a first network having a first network protocol and a second network having a second network protocol, the second network being a storage area network (see Yao et al., ¶ 4), said system comprising: a first data port for receiving first input data and first state information from said first network, said first input data being expressed in said first network protocol (see Yao et al., ¶ 6); a second data port for receiving second input data and second state information from said second network, said second input data being expressed in said second network protocol (see Yao et al., ¶ 26); a first translation system configured to translate said second input data into corresponding data expressed in said first network protocol on the basis of said first state information, the first a translation system including one or more translation devices configured to cooperate in translating said second input data into corresponding data expressed in said first network protocol (see Yao et al., ¶ 30); a second translation system configured to translate said first input data into corresponding data expressed in said second network protocol on the basis of said second state information, the second translation system including, one or more translation devices configured to cooperate in translating said first input data into corresponding data expressed in said second network protocol (see Yao et al., ¶ 150); accommodating different first and second network protocols (see Yao et al., ¶ 4). Furthermore, Satou et al. teaches a microsequencer system (see Satou et al., col. 24, lines 13-20); an instruction memory accessible to the microsequencer of the microsequencer system, said instruction memory having a plurality of instruction words (see Satou et al., col. 57, lines 18-23), each of said

instruction words forming a Very Long Instruction Word (VLIW) having a plurality of instruction fields executable in parallel by different functional units of the microsequencer (see Satou et al., col. 37, lines 29-44) to enable the microsequencer to execute a plurality of instructions in a single instruction cycle (see Satou et al., col. 34, lines 20-28). But fail to teach the instruction memory being loadable via a processor interface to make the microsequencers programmable. However, Byers et al. teaches the instruction memory being loadable via a processor interface to make the microsequencers programmable (see Byers et al., col. 30, lines 39-62 and col. 72, lines 3-24). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Yao et al. and Satou et al. to the instruction memory being loadable via a processor interface to make the microsequencers programmable because although Satou et al. does not explicitly state using a plurality of microsequencer systems including one or more microsequencers, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement the feature of using a plurality of microsequencer systems including one or more microsequencers since Yao et al. teaches a plurality of translation systems including one or more translation devices (see Yao et al., ¶ 50). And furthermore since Byers et al. teaches first and second microsequencer devices that work in a bidirectional manner and execute instructions in parallel in order to increase the rate at which access to file data is provided when the file data is not present in the main memory of a host processing system (see Byers et al., col. 5, lines 55-60).

7. As per claim 5, the above-mentioned motivation of claim 1 applies fully in order to combine Yao et al., Satou et al., and Byers et al. Byers et al., Yao et al., and Satou et al. teach an instruction-memory pointer for identifying a selected instruction word in said instruction memory (see Satou et al., col. 12, lines 14-22).

8. As per claim 15, Yao et al. teaches a system for enabling communication between a first network having a first network protocol and a second network having a second network protocol (see Yao et al., ¶ 4), said system comprising: a first input port for receiving input data from said first network (see Yao et al., 6); a second input port for receiving state information associated with said first network (see Yao et al., ¶ 26); first and second processing elements in communication with said first and second input ports (see Yao et al., ¶ 30); one of the processing elements for translating input data from said first network protocol to said second network protocol, and the other for translating input data from said second network protocol to said first network protocol (see Yao et al., ¶ 50); a system to translate input data from said first network protocol to said second network protocol or from said second network protocol to said first network protocol (see Yao et al., ¶ 62); accommodating different first and second network protocols (see Yao et al., ¶ 4). Furthermore, Satou et al. teaches an instruction memory accessible to processing element, said instruction memory having a plurality of instruction words (see Satou et al., col. 10, lines 37-49), each of said instruction words forming a Very Long Instruction Word (VLIW) having a plurality of instruction fields executable in parallel by different cooperating functional units of the processing element (see Satou et al., col. 37, lines 29-44) to enable the processing element to execute a

plurality of instructions in a single instruction cycle (see Satou et al., col. 34, lines 20-28); an instruction-memory pointer for identifying a selected instruction word in said instruction memory (see Satou et al., col. 12, lines 14-22). But fail to teach the instruction memory being loadable via a processor interface to make the functional units programmable. However, Byers et al. teaches the instruction memory being loadable via a processor interface to make the functional units programmable (see Byers et al., col. 30, lines 39-62 and col. 72, lines 3-24). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Yao et al. and Satou et al. to the instruction memory being loadable via a processor interface to make the functional units programmable since Byers et al. teaches first and second microsequencer devices that work in a bidirectional manner and execute instructions in parallel in order to increase the rate at which access to file data is provided when the file data is not present in the main memory of a host processing system (see Byers et al., col. 5, lines 55-60).

9. Claims 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yao et al., Byers et al., and Satou et al. as applied to claim 1 above, and further in view of Radogna et al. (5,991,299).

10. As per claim 6, Byers et al., Yao et al., and Satou et al. teach the mentioned limitations of claim 1 above but fail to teach a system, further comprising a translation-memory accessible to each of the microsequencers of said first and second microsequencer systems, said translation-memory having a translation-memory

address, and a translation-memory element corresponding to said translation-memory address, said translation-memory element including data for causing an instruction-memory pointer to jump to a selected instruction word. However, Radogna et al. teaches a system, further comprising a translation-memory accessible to each of the microsequencers of said first and second microsequencer systems, said translation-memory having a translation-memory address, and a translation-memory element corresponding to said translation-memory address, said translation-memory element including data for causing an instruction-memory pointer to jump to a selected instruction word (see Radogna et al., col. 9, lines 22-27). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Byers et al., Yao et al., and Satou et al. to a system, further comprising a translation-memory accessible to each of the microsequencers of said first and second microsequencer systems, said translation-memory having a translation-memory address, and a translation-memory element corresponding to said translation-memory address, said translation-memory element including data for causing an instruction-memory pointer to jump to a selected instruction word in order to control the movement of frames from an input FIFO to an output FIFO and also to control appropriate header translations as the frames are moved from the input (see Radogna et al., col. 2, lines 10-14).

11. As per claims 7-13, the above-mentioned motivation of claim 6 applies fully in order to combine Yao et al., Satou et al., Byers et al., and Radogna et al.

12. As per claim 7, Radogna et al., Byers et al., Yao et al., and Satou et al. teach a system, wherein said translation-memory element is configured to include an absolute

address of said selected instruction word (see Radogna et al., col. 9, line 29-col. 10, line 33).

13. As per claim 8, Radogna et al., Byers et al., Yao et al., and Satou et al. teach a system, wherein said translation-memory element is configured to include an offset from a current instruction word to said selected instruction word (see Radogna et al., col. 9, line 29-col. 10, line 33).

14. As per claim 9, Radogna et al., Yao et al., Byers et al., and Satou et al. teach a system, further comprising a translation-memory pointer for indirectly causing said instruction-memory pointer to jump to a selected instruction-memory address (see Radogna et al., col. 8, line 58-col. 9, line 5).

15. As per claim 10, Radogna et al., Yao et al., Byers et al., and Satou et al. teach a system, wherein said translation-memory pointer is configured to identify a selected translation-memory address corresponding to a translation-memory element that contains data indicative of said selected instruction-memory address (see Radogna et al., col. 8, line 58-col. 9, line 5).

16. As per claim 11, Radogna et al., Byers et al., Yao et al., and Satou et al. teach a system, further comprising a translation-memory having: a translation-memory address; a first translation-memory element corresponding to said translation-memory address, said first translation-memory element including data for causing an instruction-memory pointer to jump to a first instruction word (see Radogna et al., col. 9, lines 22-27); a second translation-memory element corresponding to said translation-memory address, said second translation-memory element including data for causing said instruction-

memory pointer to jump to a second instruction word (see Radogna et al., col. 15, line 65-col. 16, line 15); and a selector for selecting said first translation-memory element (see Radogna et al., col. 9, line 29-col. 10, line 33).

17. As per claim 12, Radogna et al., Byers et al., Yao et al., and Satou et al. teach a system, wherein said selector comprises a multiplexer having a first multiplexer input for receiving data indicative of content of said first translation-memory element; a second multiplexer input for receiving data indicative of content of said second translation-memory element (see Radogna et al., col. 5, lines 50-64); an output providing data selected from at least said first multiplexer input and said second multiplexer input; and a control input for controlling data provided at said output (see Radogna et al., col. 9, line 29-col. 10, line 33).

18. As per claim 13, Radogna et al., Byers et al., Yao et al., and Satou et al. teach a system, further comprising an output port in communication with said second microsequencer system for providing said corresponding data to said second network (see Radogna et al., col. 12, lines 27-41).

19. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yao et al., Byers et al., and Satou et al. as applied to claims 1 and 15 above, and further in view of Muller et al. (6,453,360).

20. As per claim 14, Yao et al., Byers et al., and Satou et al. teach the mentioned limitations of claim 1 above but fail to teach a system, wherein said first and second data ports and said first and second microsequencer systems are integrated into one

integrated circuit. However, Muller et al. teaches a system, wherein said first and second data ports and said first and second microsequencer systems are integrated into one integrated circuit (see Muller et al., col. 8, lines 10-20). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Yao et al., Byers et al., and Satou et al. to a system, wherein said first and second data ports and said first and second microsequencer systems are integrated into one integrated circuit in order to increase the efficiency of handling network traffic (see Muller et al., col. 4, lines 21-31).

21. As per claim 16, Yao et al., Byers et al., and Satou et al. teach the mentioned limitations of claim 15 above but fail to teach a system wherein said first and second processing elements are selected from the group consisting of: a micro-processor; and an application-specific integrated circuit. However, Muller et al. teaches a system wherein said first and second processing elements are selected from the group consisting of: a micro-processor; and an application-specific integrated circuit (see Muller et al., col. 8, lines 10-20 and col. 24, lines 12-25). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Yao et al., Byers et al., and Satou et al. to a system wherein said first and second processing elements are selected from the group consisting of: a micro-processor; and an application-specific integrated circuit in order to capitalize on the increased processor resources that are available in multi-processor computer systems (see Muller et al., col. 3, lines 29-42).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ranodhi Serrao whose telephone number is (571)272-7967. The examiner can normally be reached on 8:00-4:30pm, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia can be reached on (571)272-3880. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RUPAL DHARIA
SUPERVISORY PATENT EXAMINER